Silicon Amnesia and Dementia:

Radiation effects in microelectronics

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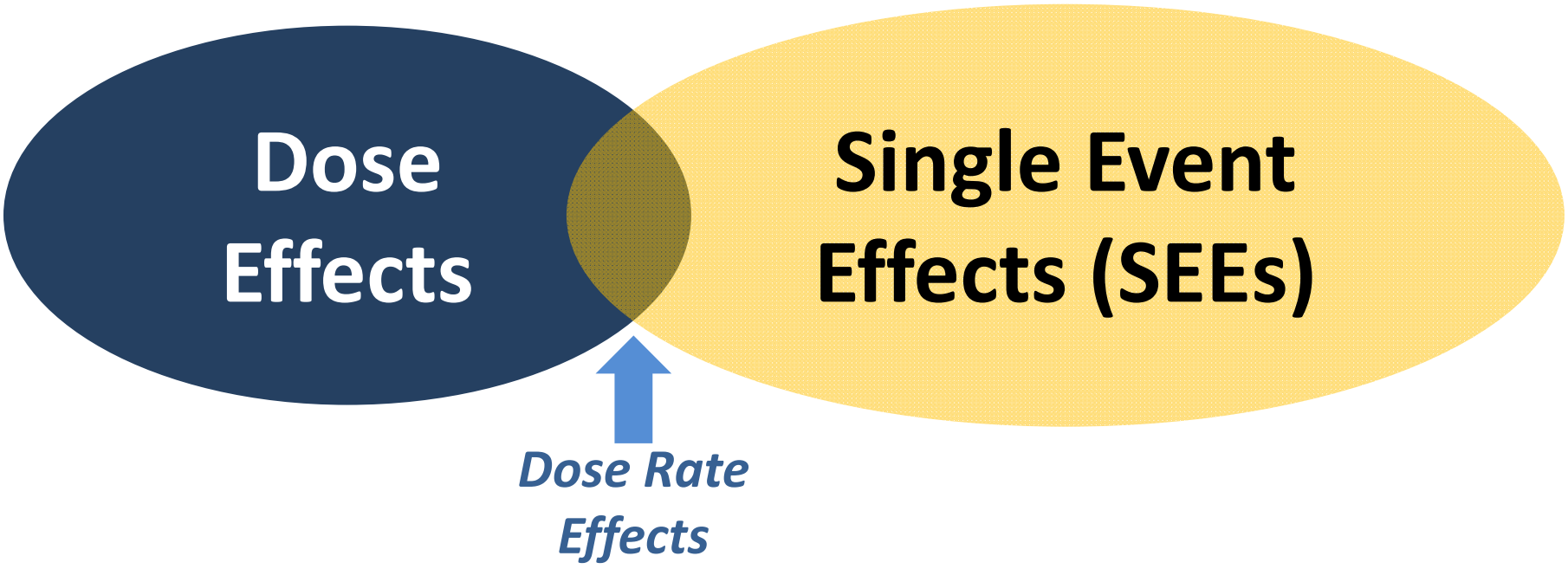
Outline

- Radiation & Environments
- Key Effects: Chronic vs. One-shot
- Impact of Technology Scaling
- Intentional Mitigation
- Summary

What Radiation DOES in Matter

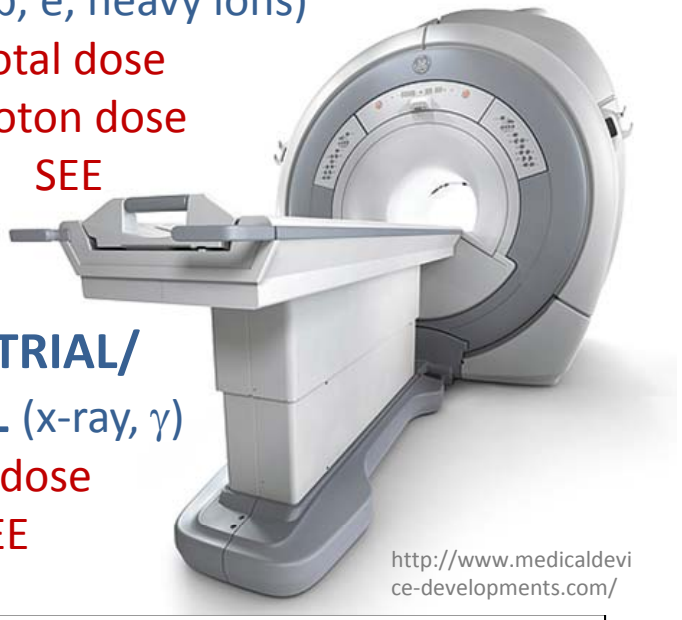
- Transient Charge Generation (direct ionization)
- Structural Damage (displacement damage)
- Nuclear Reactions (secondary production)




Wikimedia ("Upshot-Knothole GRABLE")

TERRESTRIAL (α, n)
SEE

SPACE (p, e, heavy ions)
total dose
proton dose
SEE

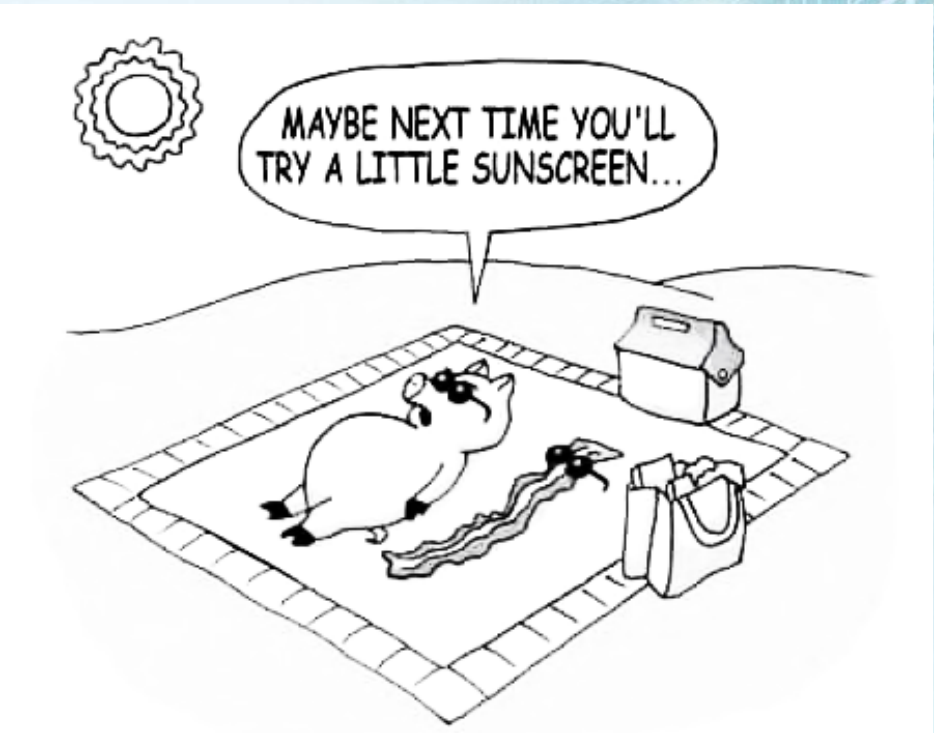

http://www.medicaldevice-developments.com/

MILITARY (γ, n)
dose-rate
total dose
neutron dose
SEE

INDUSTRIAL/ MEDICAL (x-ray, γ)
total dose
SEE

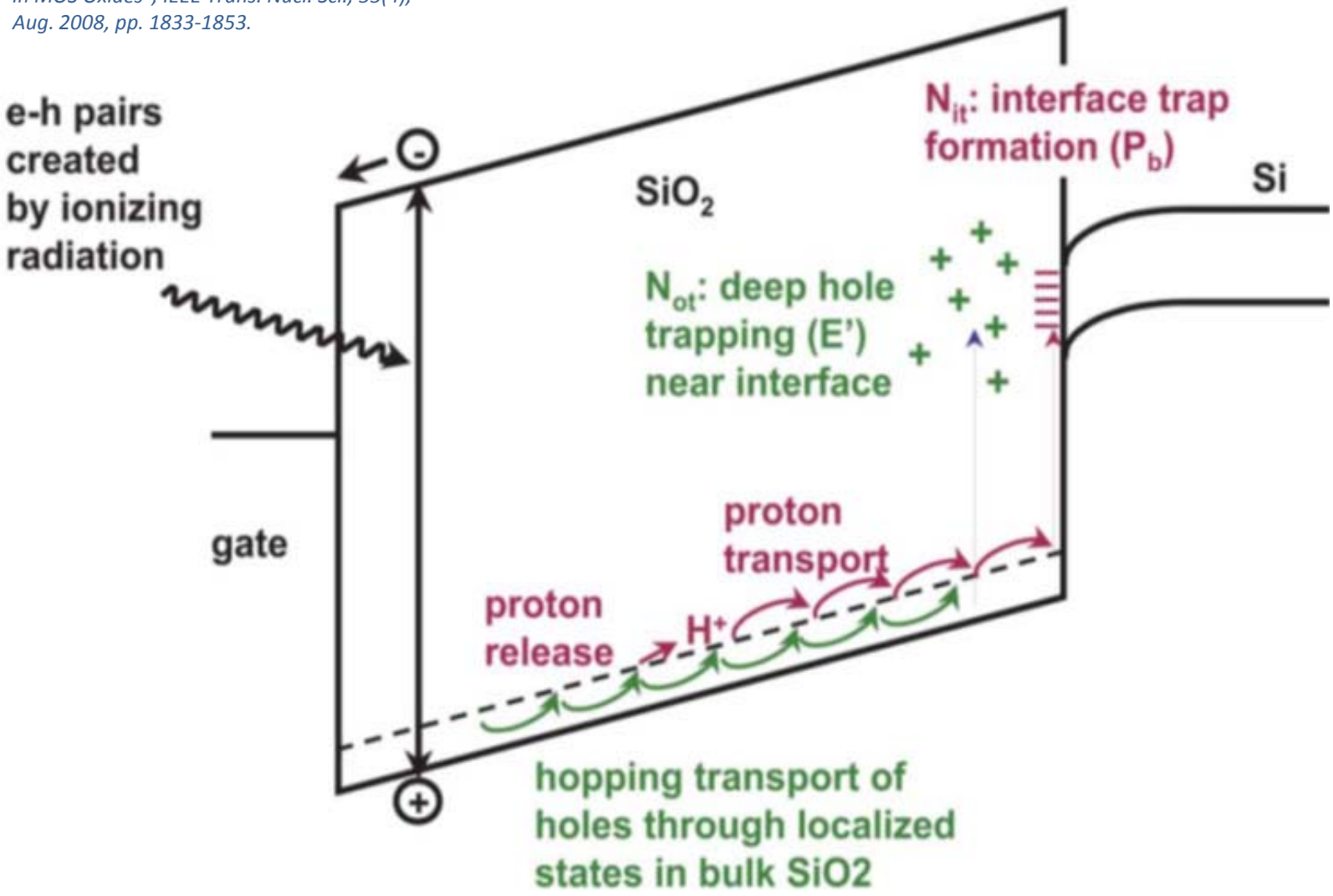
Total Ionizing Dose (TID)

- Accumulated rad exposure (chronic) over time
- Absorbed dose is in the oxides/insulators
- Device parameters shift as a function of dose
- Parameter shifts are quasi-permanent

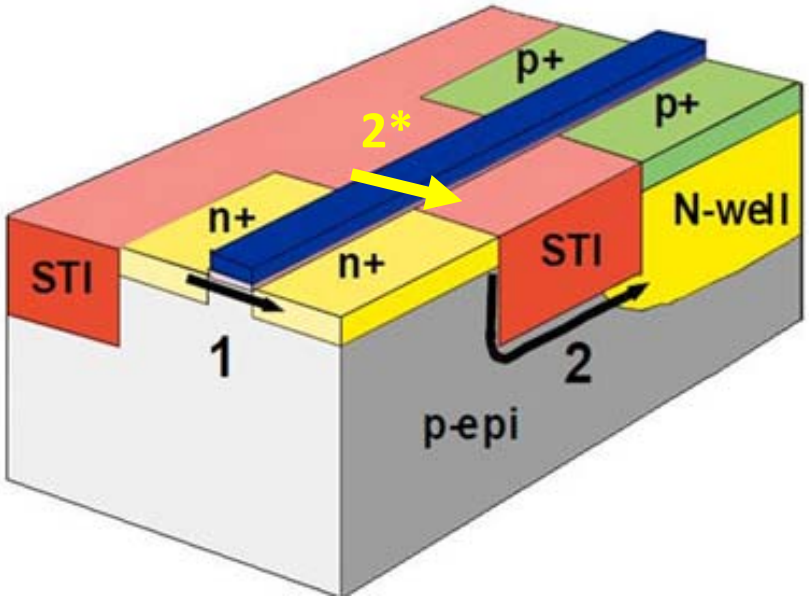


TID – Hole Trapping & Transport

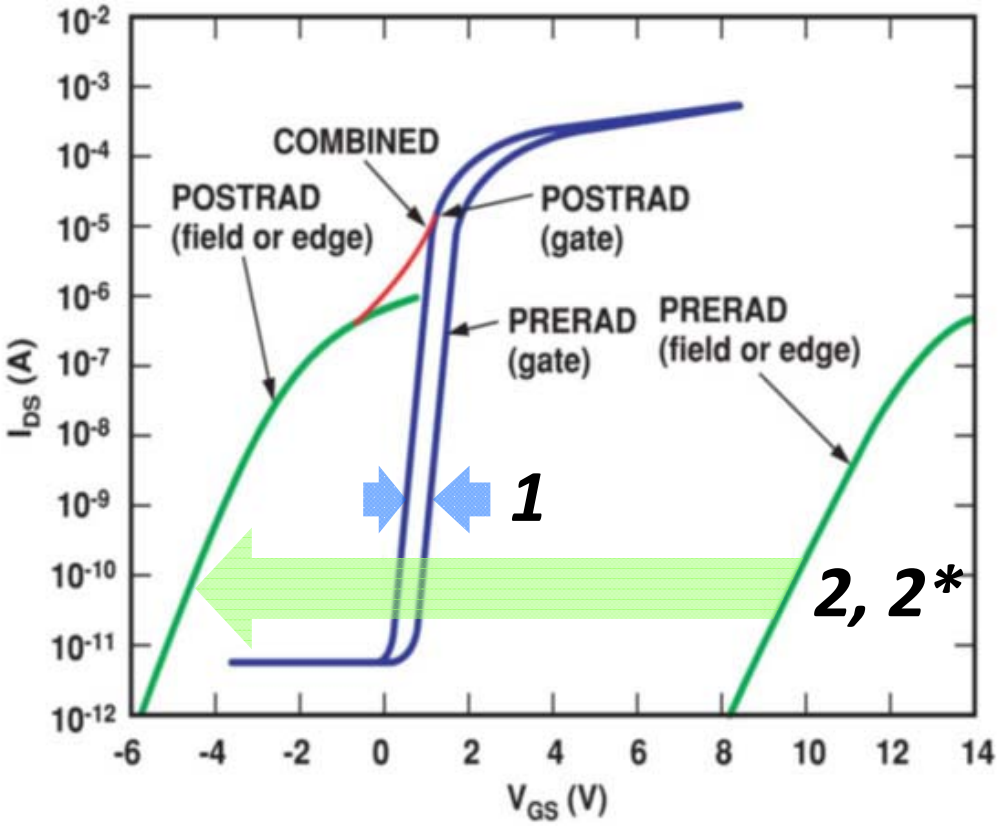
James R. Schwank et al., "Radiation Effects in MOS Oxides", IEEE Trans. Nucl. Sci., 55(4), Aug. 2008, pp. 1833-1853.



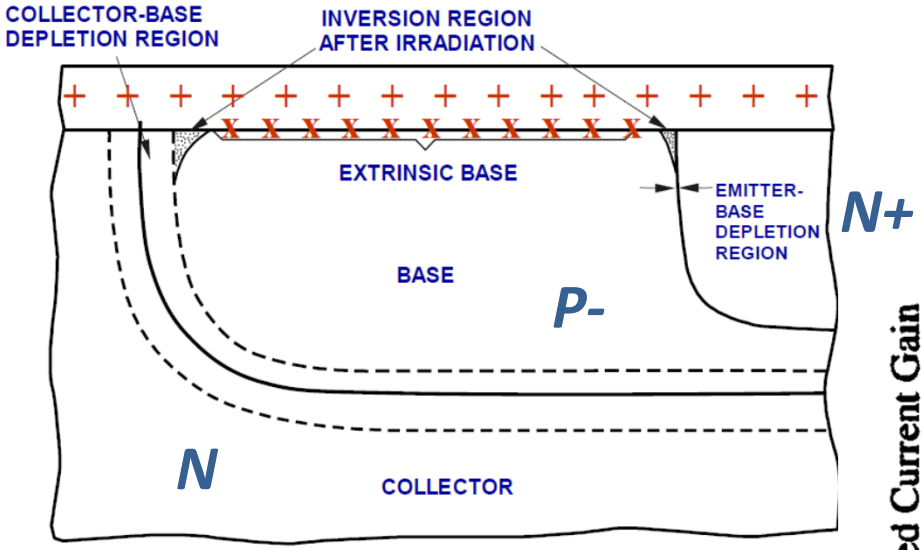
TID in MOS Transistors



James R. Schwank et al., "Radiation Effects in MOS Oxides", IEEE Trans. Nucl. Sci., 55(4), Aug. 2008, pp. 1833-1853.



TID in Bipolar Transistors

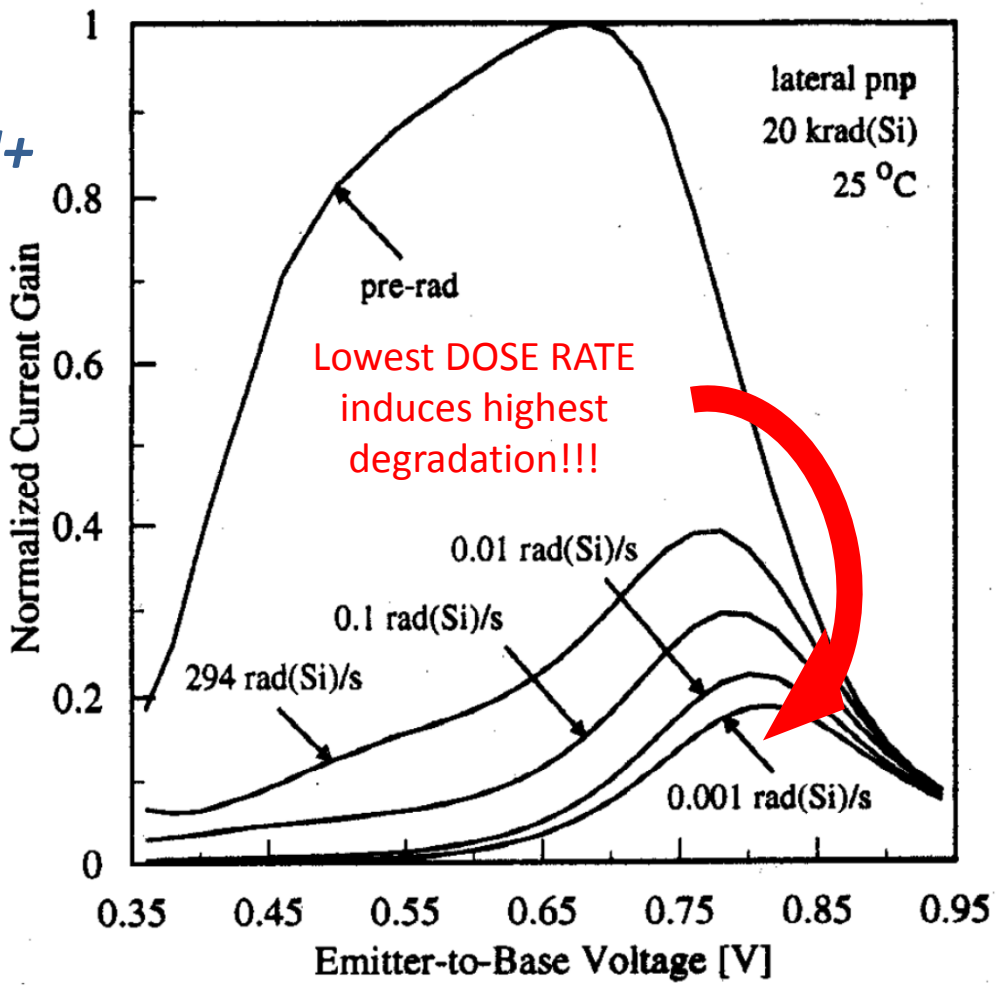


From http://parts.jpl.nasa.gov/docs/Radcrs_Final.pdf

$$I_B \sim R_{surface}$$

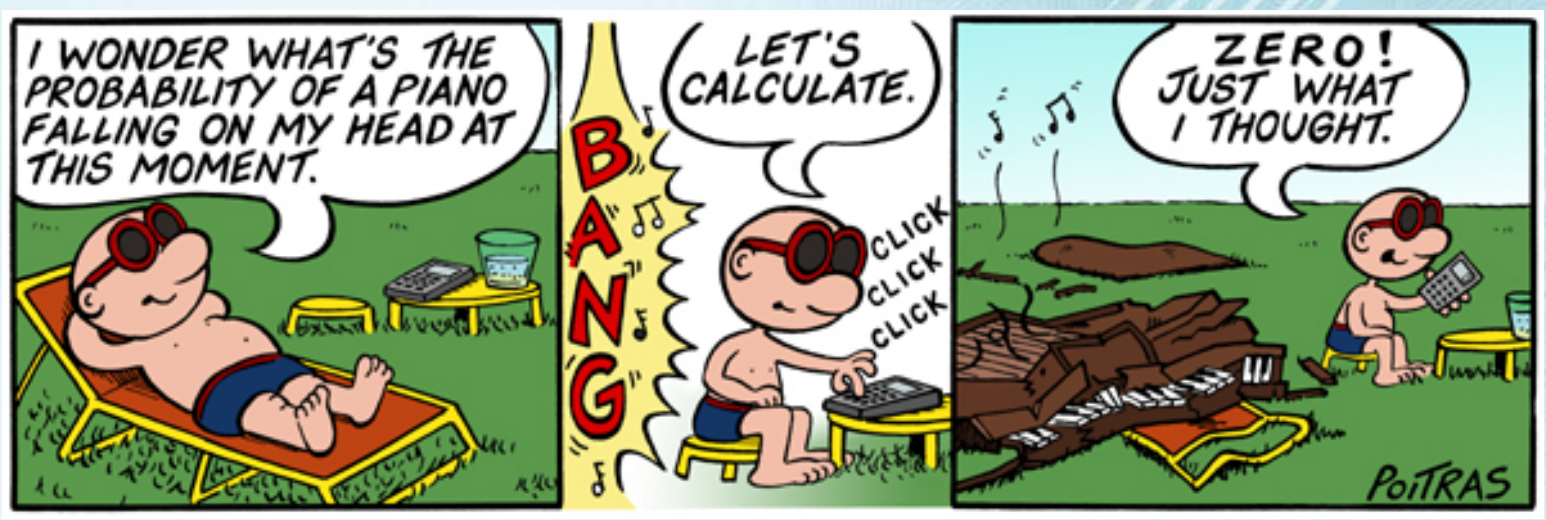
$$\downarrow \beta = \frac{I_C}{I_B \uparrow}$$

S. Witczak, et al., "Accelerated tests for simulating low dose rate gain degradation of lateral and substrate pnp bipolar junction transistors," Trans. Nucl. Sci. 43(6), Dec. 2014, pp. 3151-61.



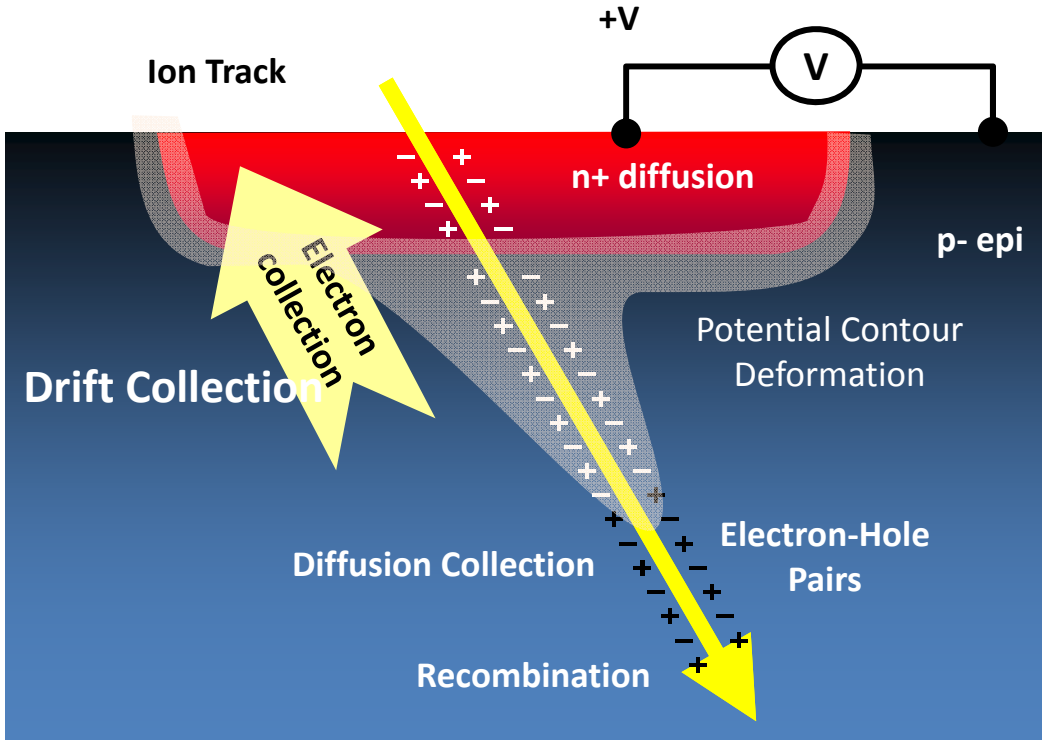
Single Event Effects (SEEs)

- Individual event creates a transient
- Transient upsets downstream circuits or causes bit flips in memory/sequentials
- Stochastic (random spatially and in time)
- Typically a rare event (1 per month, etc.)

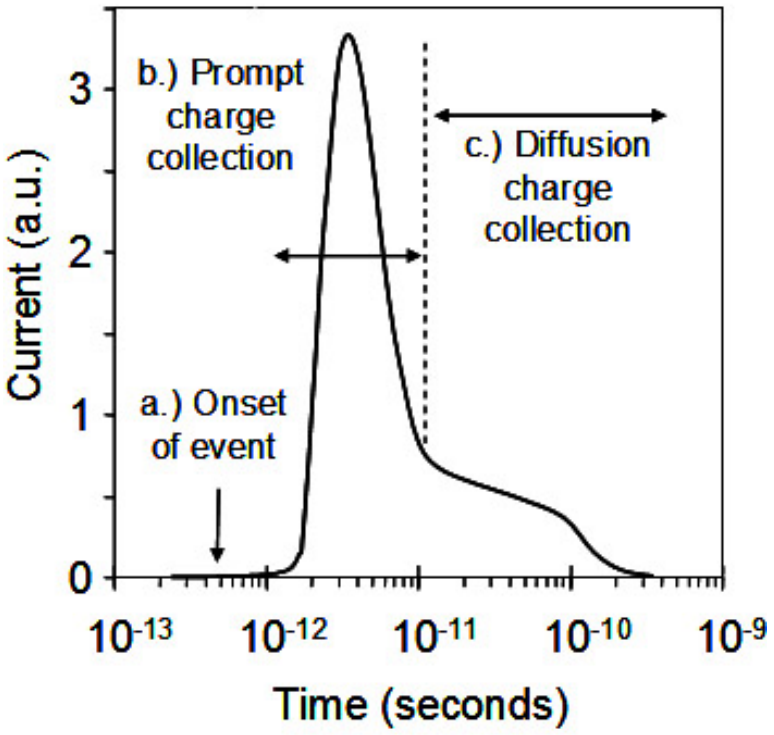


From http://toonut.com/piano-falling-from-sky-probability/

The Ubiquitous “Radiation Detector”

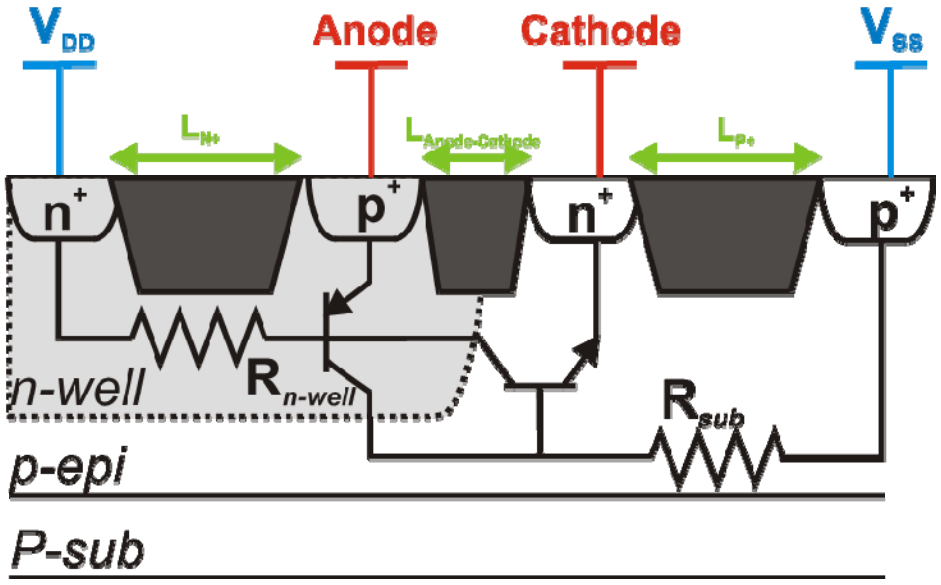


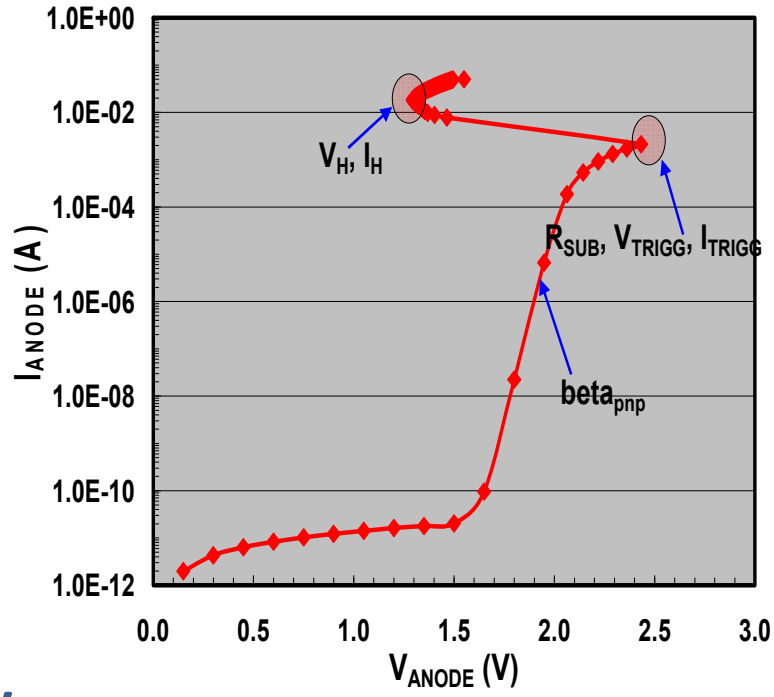
Reverse-biased N+/P junction



SET => SEU, SBU, MBU, SEFI, SEL…

CMOS Single Event Latchup (SEL)

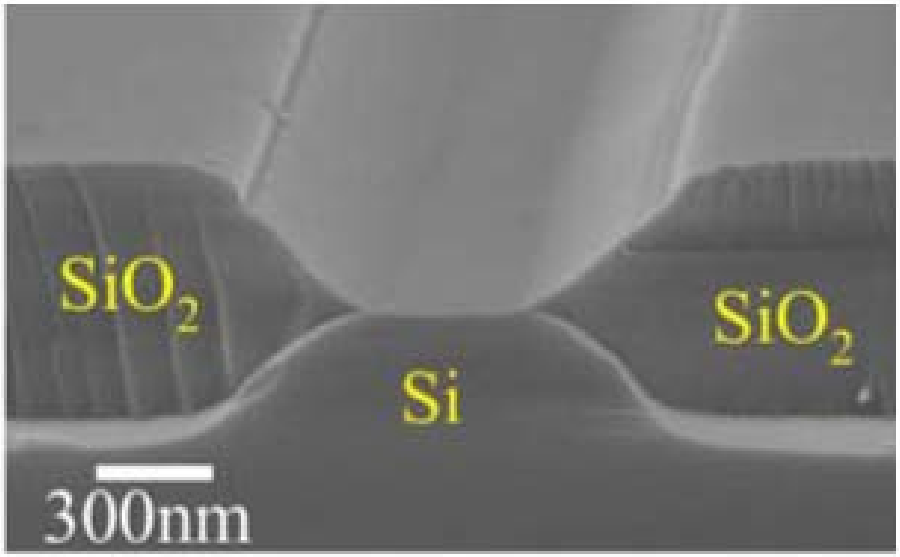


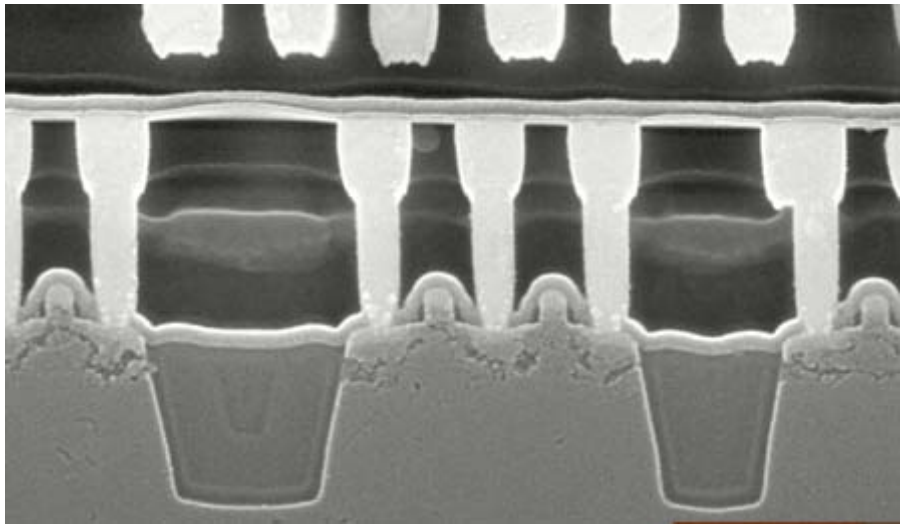


- Circuit fails functionality
- SCR causes higher current (Latched state)
- "Latch" can only be removed by power cycling
- Can be destructive at high currents

Incidental radiation tolerance due to Technology Scaling

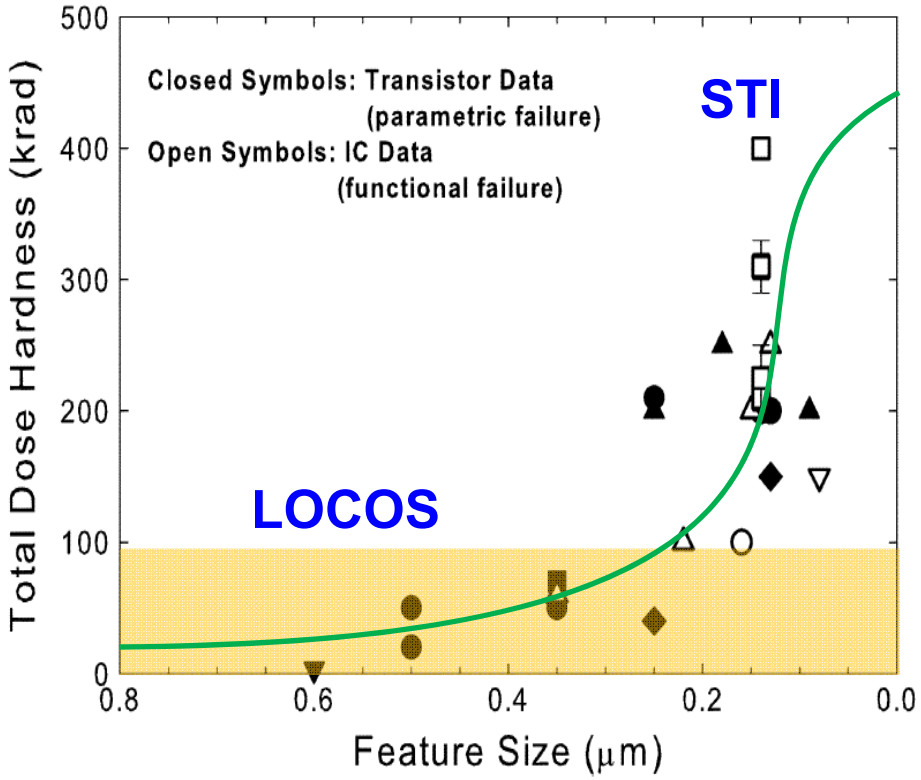
TID vs. Isolation Oxide Type





http://www.chipworks.com/

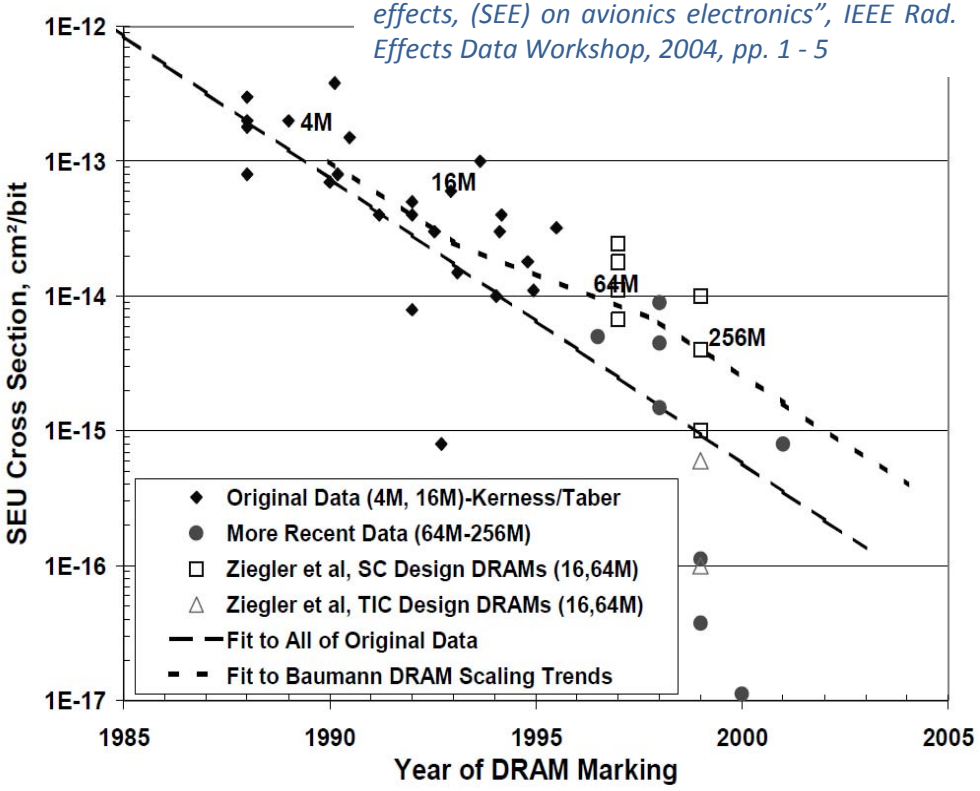
P. Dodd, M. Shaneyfelt, J. Schwank, J. Felix, "Current and Future Challenges in Radiation Effects on CMOS Electronics", IEEE Trans. Nuclear Science, 57(4) , Part: 1, August 2010, pp. 1747 - 1763

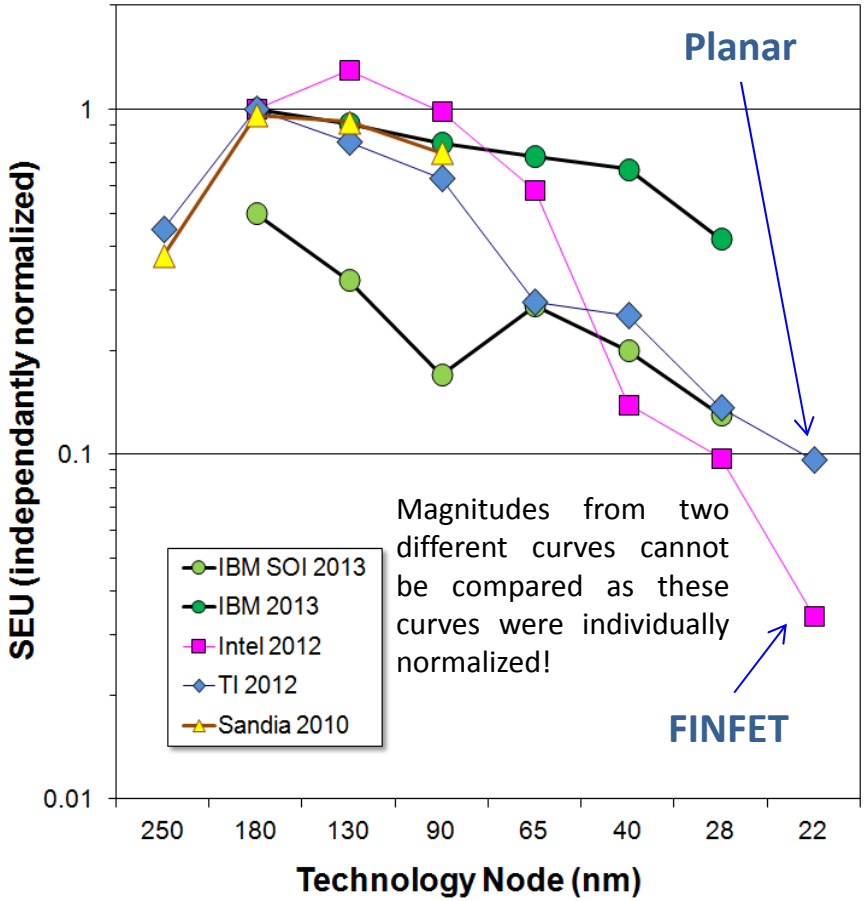


SRAM/DRAM Bit SEU vs. Scaling

DRAM bit sensitivity has been decreasing with scaling

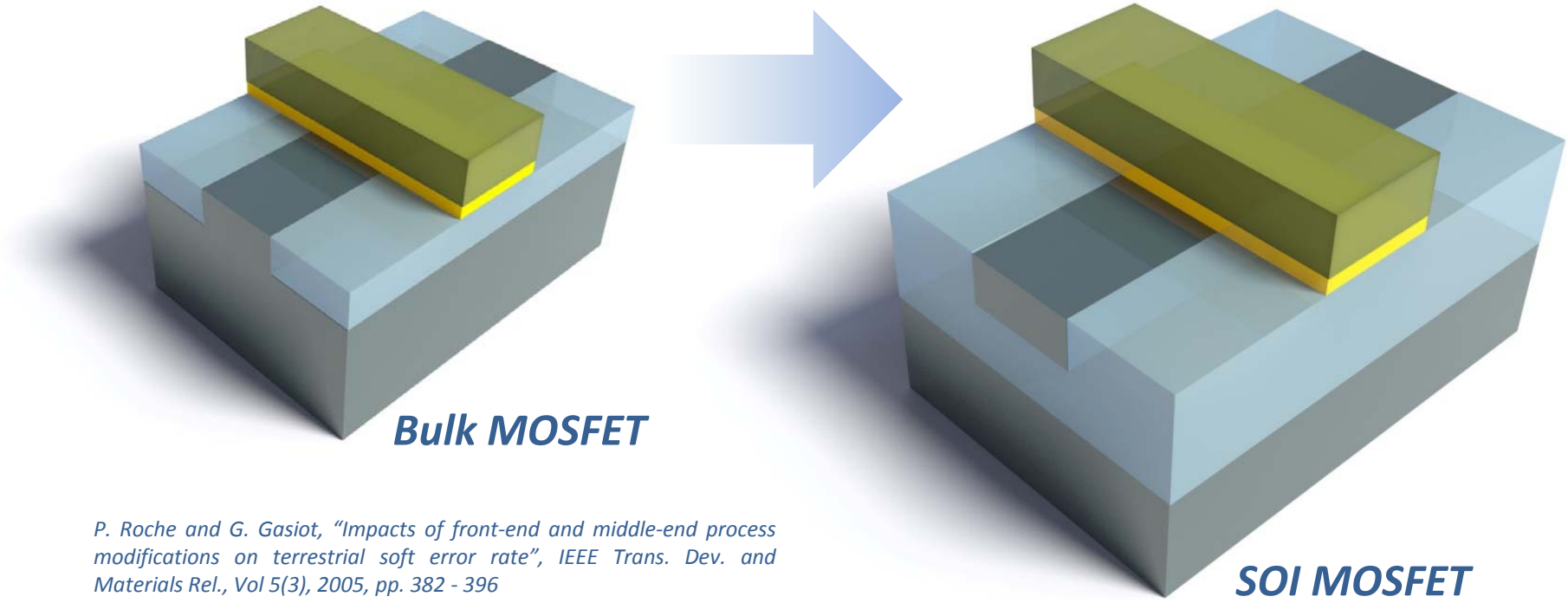
R. H. Edwards, C. S. Dyer, E. Normand, "Technical standard for atmospheric radiation single event effects, (SEE) on avionics electronics", IEEE Rad. Effects Data Workshop, 2004, pp. 1 - 5





SRAM bit sensitivity has been decreasing with scaling (since the 130nm node)

Silicon on Insulator (SOI)



Bulk MOSFET

SOI MOSFET

P. Roche and G. Gasiot, "Impacts of front-end and middle-end process modifications on terrestrial soft error rate", IEEE Trans. Dev. and Materials Rel., Vol 5(3), 2005, pp. 382 - 396

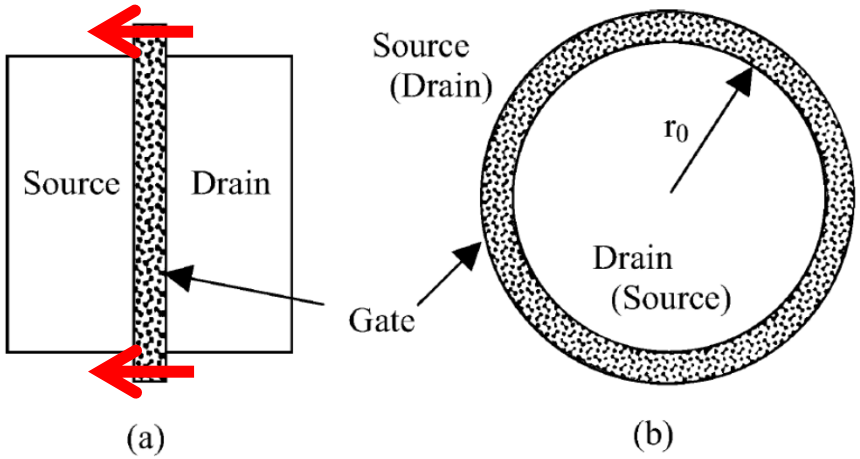
Process Option	Relative SER
Bulk General Purpose	100
Bulk Low Power	90
Triple/Deep N-Well	60–75
Body tied PD SOI	< 1
Floating body PD SOI	15–20
FD SOI	10

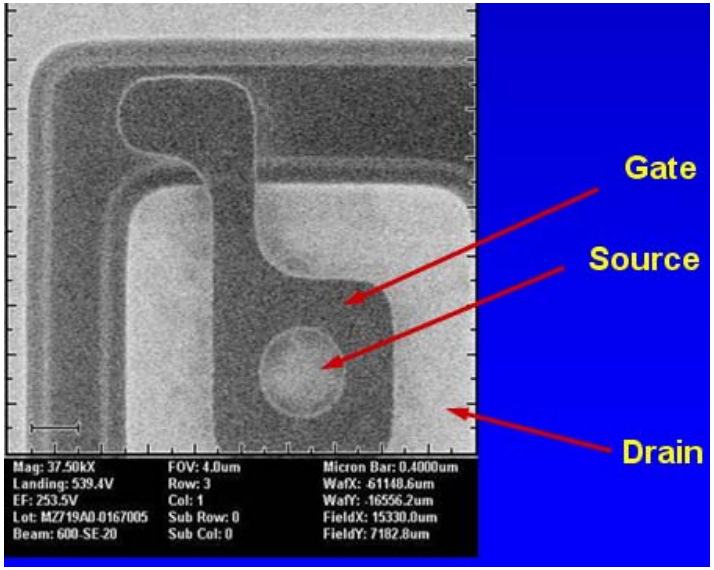
Eliminates SEL and reduces SEU by 4x – 10x

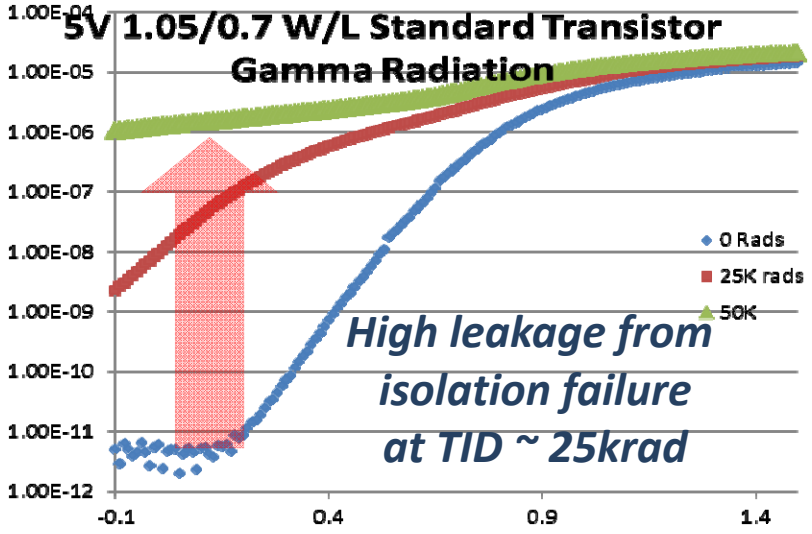
“Intended” Mitigation: Radhard by Design/Process

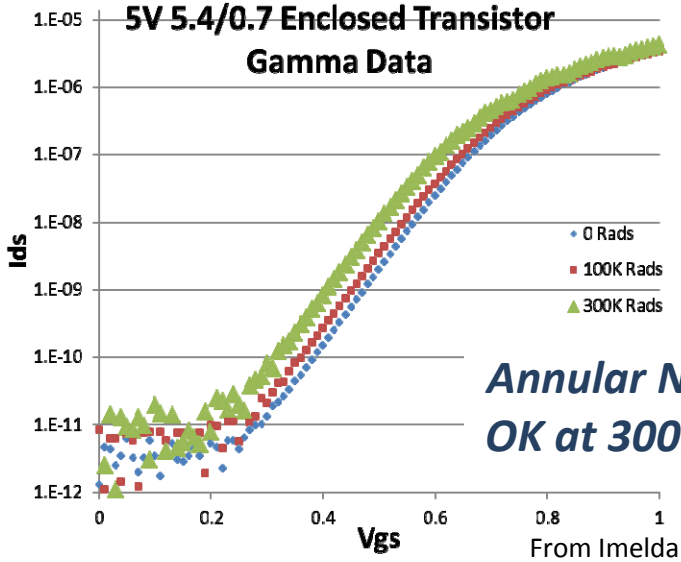
Annular "Edgeless" MOSFET

D. C. Mayer, et al., "Reliability Enhancement in High-Performance MOSFETs by Annular Transistor Design", IEEE Trans. Nuc. Sci, 51(6), Dec. 2004, pp. 3615-20



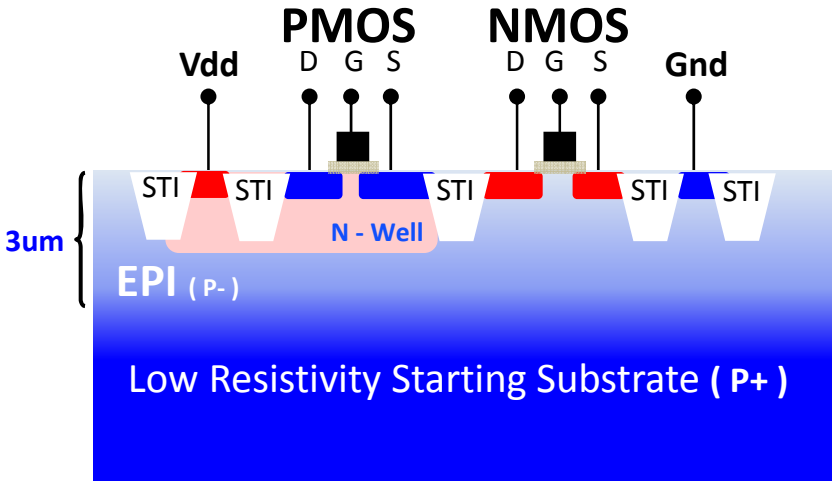


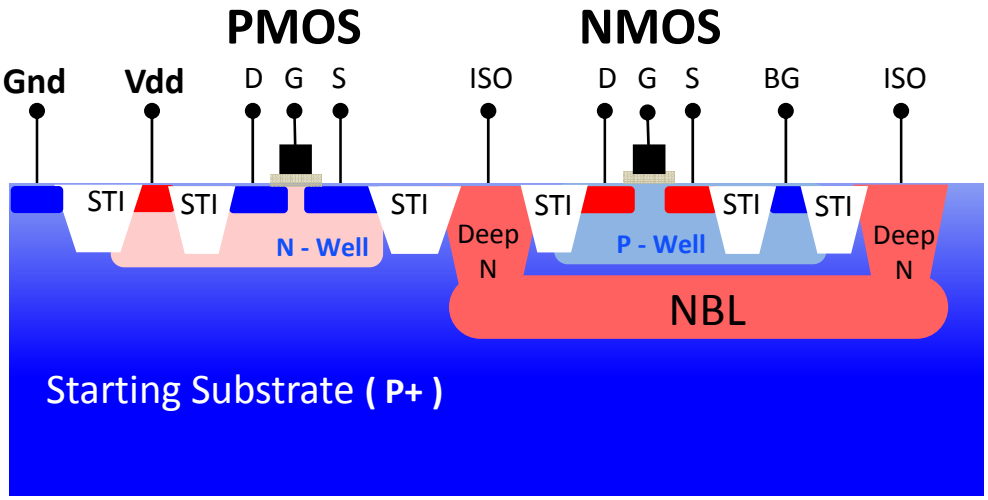




From Imelda Donnelly

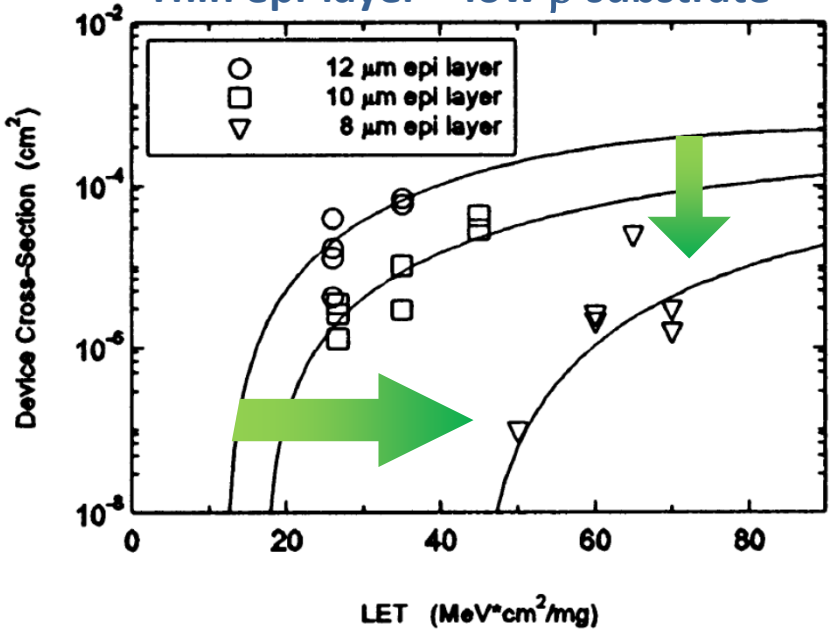
Improving Latch-up Tolerance





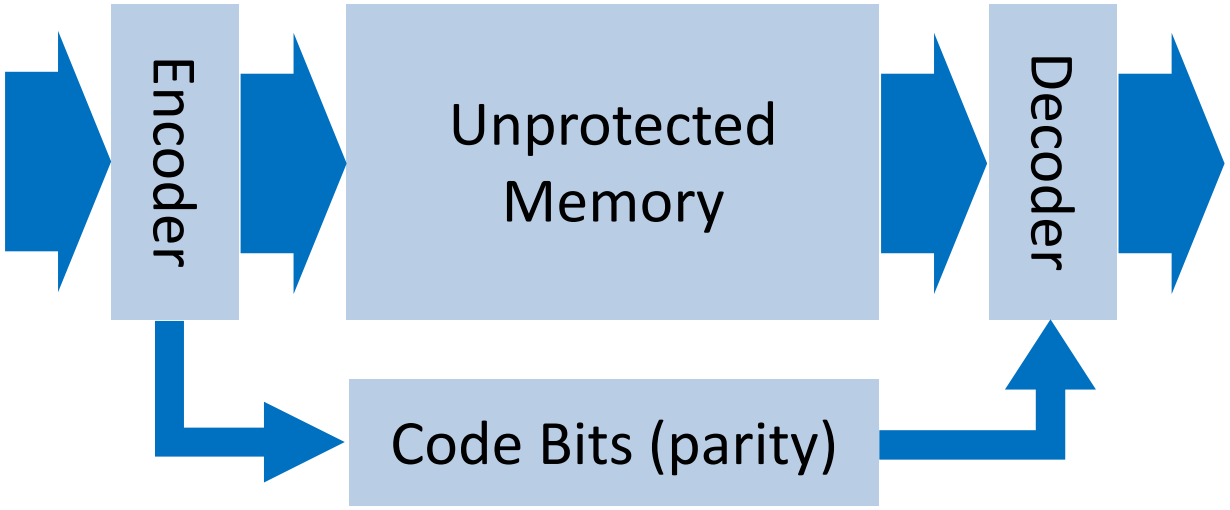
buried isolation layers

Thin epi-layer + low ρ substrate



K. LaBel, et al., "Single event effect characteristics of CMOS devices employing various epi-layer thicknesses", RADECS, Sept. 1995., pp. 258- 262

Memory Error Correction (ECC)



	SEC-DED			SBC-DBD (B=4 bits)			DEC-TED		
Data Bits	check bits	over-head	Total Bits	check bits	over-head	Total Bits	check bits	over-head	Total Bits
16	6	38%	22	12	75%	28	11	69%	27
32	7	22%	39	12	38%	44	13	41%	45
64	8	13%	72	14	22%	78	15	23%	79
128	9	7%	137	16	13%	144	17	13%	145

ECC reduces SEU by > 1000x

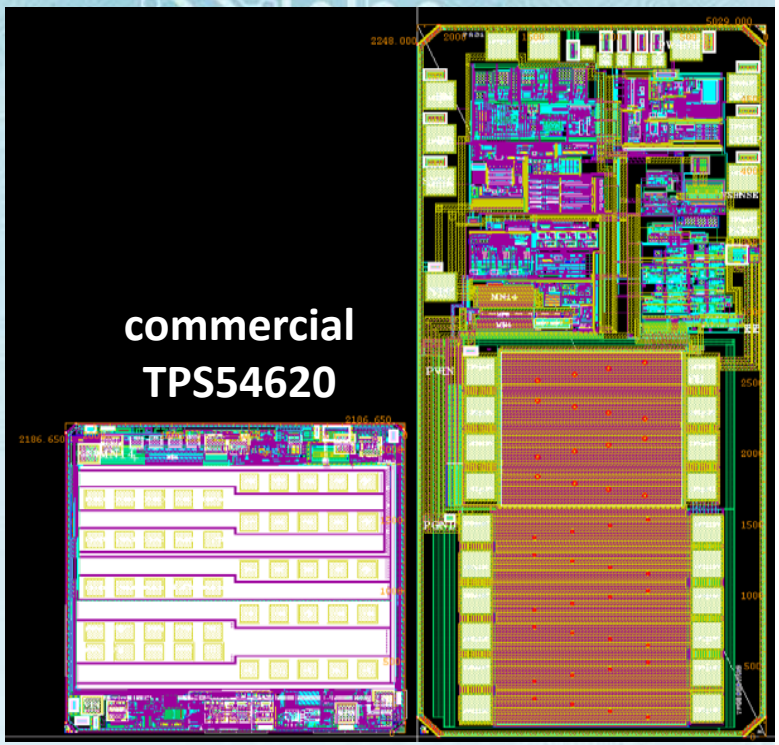
C. Slayman, "Cache and memory error detection, correction, and reduction techniques for terrestrial servers and workstations", IEEE Trans. on Device and Materials Reliability, Vol. 5(3), 2005, pp. 397 - 404

Concluding Remarks

- Electronics are plagued by chronic dose effects (dementia) and single-event effects (amnesia) in rad. environments. These two processes, working alone, or, in concert, limit system reliability.

- Scaling has improved the radiation tolerance of more recent electronics. This serendipitous radiation tolerance is adequate for some applications.

- Dedicated rad-hardened technology is required for critical applications. Implemented via process, circuit, and architectural changes radhard tweaks impact performance and cost as compared with commercial devices.



C. Parkhurst, M. Hamlyn, and R. Khanna, "Buck Converter Design for Harsh Environments", 2012 Analog Tech. Conf., 1/11/12, p. 15